SY-MN1319X1

SY-MN1313Y1

BLE Module User Manual

- DATE OF ISSUE: 2013/11/15
- PRODUCT: Bluetooth Low Power Module
- MODEL: SY-MN1319X1 (Antenna Embedded), SY-MN1313Y1 (None Antenna)
- Rev. : V0.4

History

Version	Comment
0.1	First Draft
0.2	Update pin out description
0.3	Update pin define
0.4	Add SMT pads , RF test data , Solder temperature profile , Ref. Schematic

Approval	Check	Design

1. Key Features

True single-chip BLE SoC solution

• Integrated BLE radio
• Complete BLE protocol stack and application profiles
• Flexible analog/digital sensor interface
• Fast MCU with Flash memory to run applications
• Support both master and slave modes

Microcontroller

• Integrated 32-bitARM Cortex M0 MCU
• 256KB system memory
• 16KB RAM size
• User controllable code protection
• External application processor interface

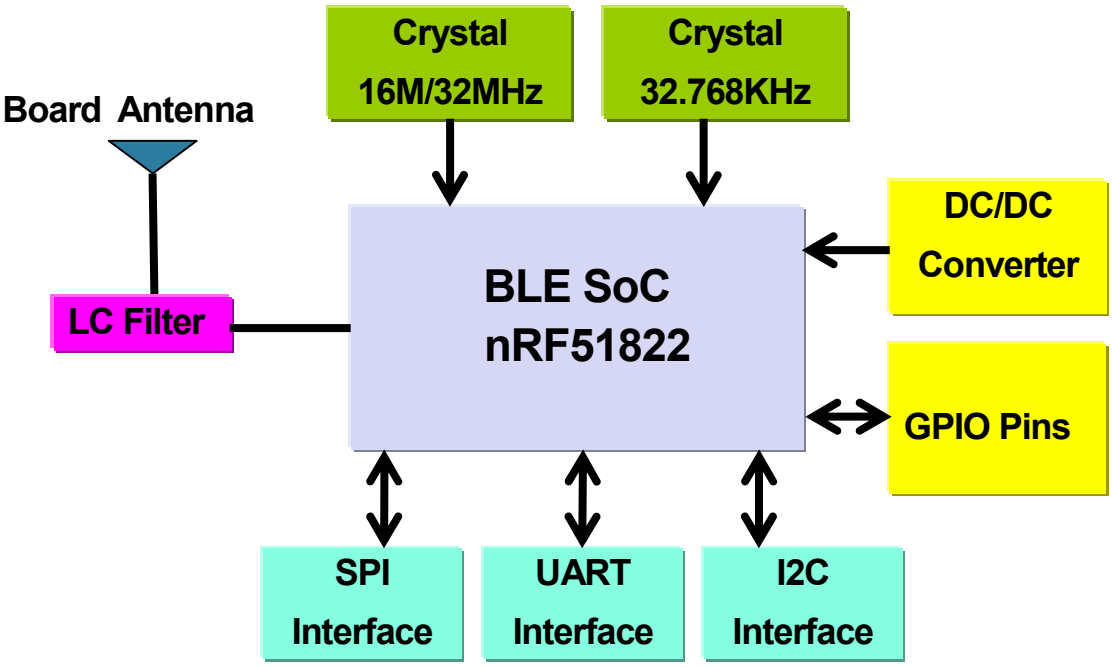
High level integration

• 8-channel 10-bit general purpose ADC
• One 32bits & two 16bits Timer with counter mode
• 31 GPIO pins
• GPIO pins can be used as interrupt sources
• Four general purpose timers
• CPU independent Programmable Peripheral Interconnect (PPI)
• Real timer counter (RTC)
• Quadrature Decoder (QDEC)
• SPI Master
• Two Wire Master I2C compatible
• UART (CTS/RTS)
• AES HW encryption
• 16/32-MHz crystal oscillator
• 32.768-kHz crystal oscillator

2. Typical Applications

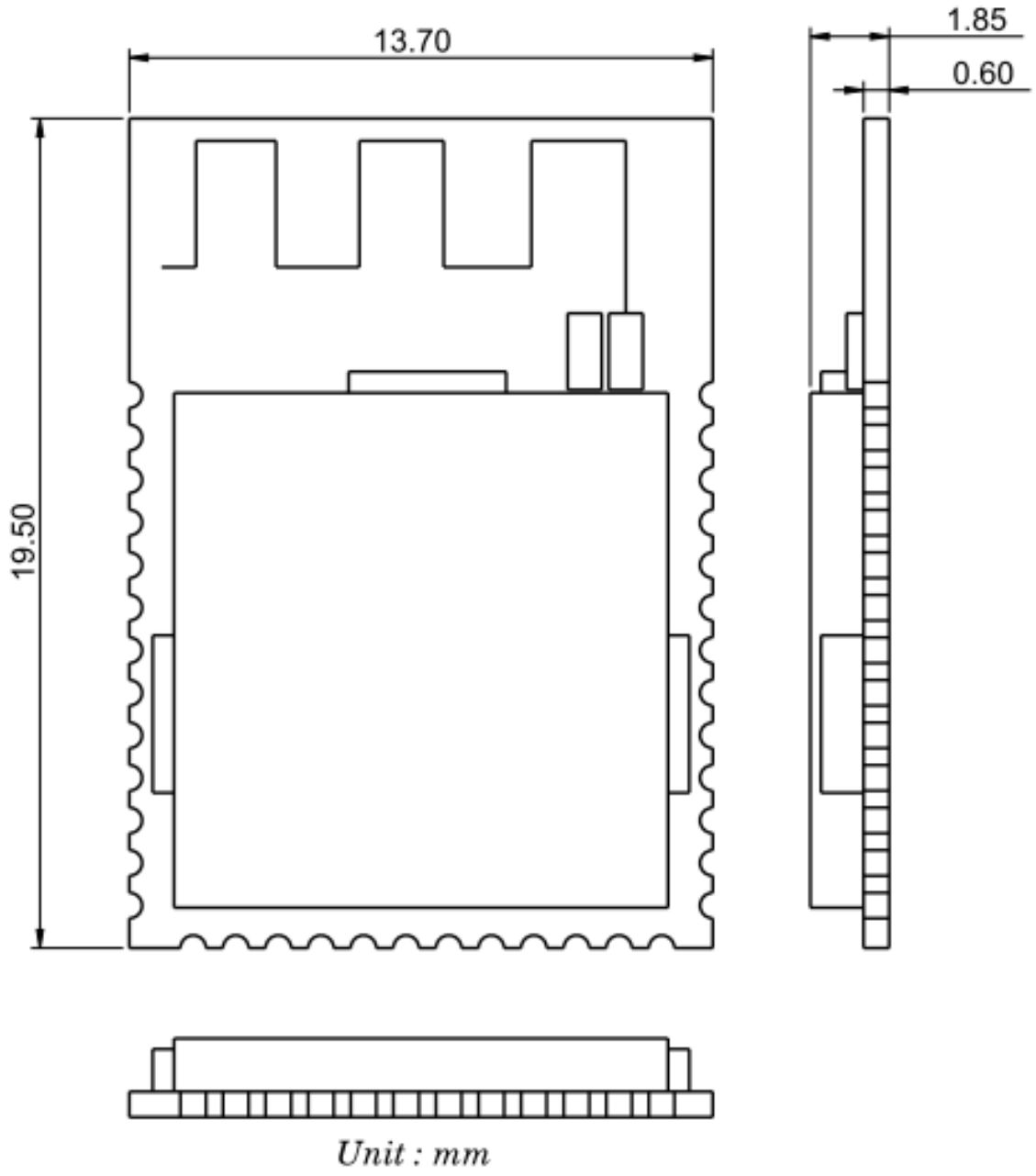
• Sports & Fitness
• Healthcare & medical
• Remote control
• Smart phone accessories
• PC peripherals (mouse, keyboard)
• Wireless Sensor networks
• 3D Glasses
• Key-fobs + Wrist Watch
• Monitor Devices
• Gaming controller
• Multi- touch track pad

3. Hardware Block Diagram

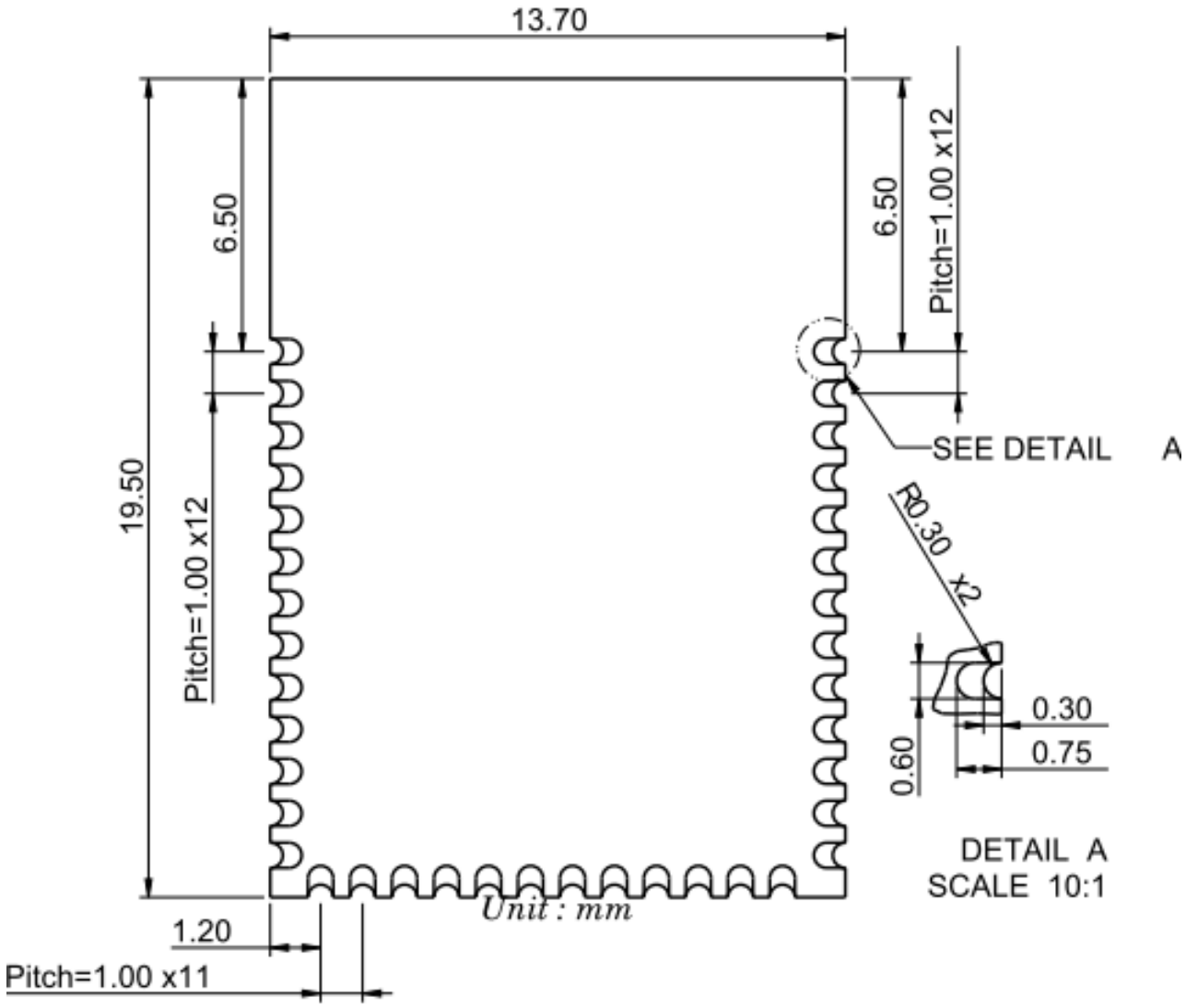


4. Package Mechanical Drawing & Dimension

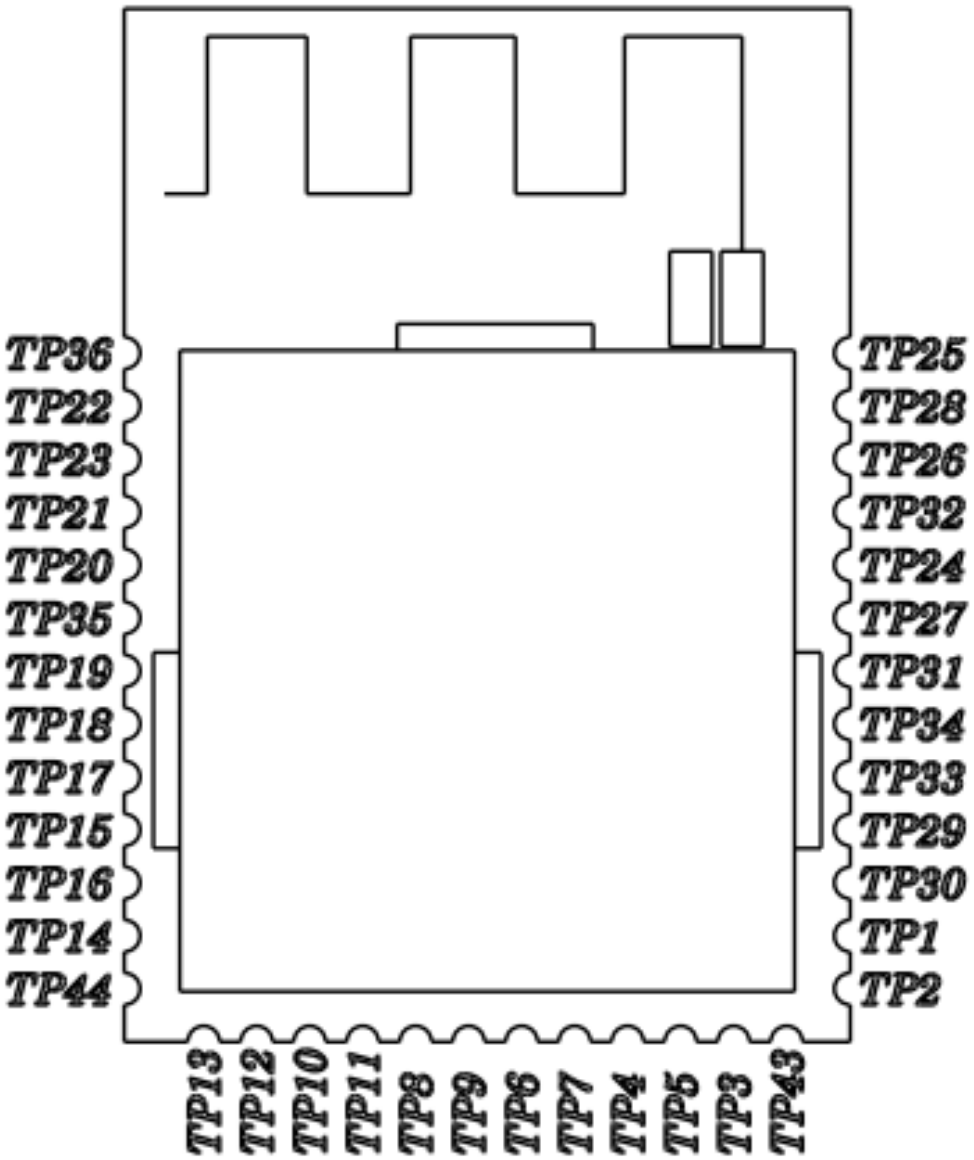
Top View



Bottom View


13.70
6.50
6.50
Pitch=1.00 x12
19.50
Pitch=1.00 x12
SEE DETAIL A
R0.30 x2
0.30
0.75
0.60
DETAIL A
SCALE 10:1
Unit : mm
1.20
Pitch=1.00 x11

5. Pins Assignment



6. Pin Assignment Description

Pins	Name	Function	Description
TP1	Vcc_nRF	Power	System Power
TP2	GND	GND	GND Pad
TP3	P0.00	I/O	General purpose I/O pin / ADC reference voltage
TP4	P0.01	I/O	General purpose I/O pin / ADC input 2
TP5	P0.02	I/O	General purpose I/O pin / ADC input 3
TP6	P0.03	I/O	General purpose I/O pin / ADC input 4
TP7	P0.04	I/O	General purpose I/O pin / ADC input 5
TP8	P0.05	I/O	General purpose I/O pin / ADC input 6
TP9	P0.06	I/O	General purpose I/O pin
TP10	P0.07	I/O	General purpose I/O pin
TP11	P0.08	I/O	General purpose I/O pin
TP12	P0.09	I/O	General purpose I/O pin
TP13	P0.10	I/O	General purpose I/O pin
TP14	P0.11	I/O	General purpose I/O pin
TP15	P0.12	I/O	General purpose I/O pin
TP16	P0.13	I/O	General purpose I/O pin
TP17	P0.14	I/O	General purpose I/O pin
TP18	P0.15	I/O	General purpose I/O pin
TP19	P0.16	I/O	General purpose I/O pin
TP20	P0.17	I/O	General purpose I/O pin
TP21	P0.18	I/O	General purpose I/O pin
TP22	P0.19	I/O	General purpose I/O pin
TP23	P0.20	I/O	General purpose I/O pin
TP24	P0.21	I/O	General purpose I/O pin
TP25	P0.22	I/O	General purpose I/O pin
TP26	P0.23	I/O	General purpose I/O pin
TP27	P0.24	I/O	General purpose I/O pin
TP28	P0.25	I/O	General purpose I/O pin
TP29	GND	I/O	GND Pad
TP30	P0.27	I/O	32.768KHz installed, Disconnect all to this Pin.
TP31	P0.28	I/O	General purpose I/O pin
TP32	P0.29	I/O	General purpose I/O pin
TP33	P0.30	I/O	General purpose I/O pin
TP34	P0.31	I/O	General purpose I/O pin
TP35	SWDIO/nReset	I/O	System Reset (Active Low) Also HW debug and flash programming I/O
TP36	SWD CLK	I/O	HW debug and flash programming I/O
TP43	GND	GND	GND Pad
TP44	GND	GND	GND Pad
TP40	RF	TX/RX	ANT Feed port (only for None antenna version)

PS. All I/O pin can re-configure at any function, like SPI, I2C and GPIO in / out application. Except the ADC function must use ADC dedicate pin.

7. Electrical Specifications

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
VCC_nRF	Supply voltage	VCC to GND	-0.3	+3.6	V
Ts	Storage temperature		-40	+125	℃
ESD	Human-body model	REN,RFP		1.5	KV
		Other pads	2		KV
	Machine model	All pads	200		V
	Charge-device model	All pads	500		V

Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
VCC_nRF	Power Supply	Relative to GND	1.8	3.0	3.6	V
T A	Operating temperature		-25	25	+70	℃

DC Characteristics

Symbol	Description	Note	Min.	Typ.	Max.	Units	Test level
$I_{TX,+4dBm}$	TX only run current @ P_{OUT} = +4 dBm	1		16		mA	4
$I_{TX,0dBm}$	TX only run current @ P_{OUT} = 0 dBm	1		10.5		mA	4
$I_{TX,-4dBm}$	TX only run current @ P_{OUT} = -4 dBm	1		8		mA	2
$I_{TX,-8dBm}$	TX only run current @ P_{OUT} = -8 dBm	1		7		mA	2
$I_{TX,-12dBm}$	TX only run current @ P_{OUT} = -12 dBm	1		6.5		mA	2
$I_{TX,-16dBm}$	TX only run current @ P_{OUT} = -16 dBm	1		6		mA	2
$I_{TX,-20dBm}$	TX only run current @ P_{OUT} = -20 dBm	1		5.5		mA	2
$I_{TX,-30dBm}$	TX only run current @ P_{OUT} = -30 dBm	1		5.5		mA	2
$I_{START,TX}$	TX startup current	2		7		mA	1
$I_{RX,250}$	RX only run current @ 250 kbps			12.6		mA	1
$I_{RX,1M}$	RX only run current @ 1 Mbps			13		mA	4
$I_{RX,2M}$	RX only run current @ 2 Mbps			13.4		mA	1
$I_{START,RX}$	RX startup current	3		8.7		mA	1

1. Valid for data rates 250 kbps, 1 Mbps, and 2 Mbps
2. Average current consumption (at 0 dBm TX output power) for TX startup (130 µs), and when changing mode from RX to TX (130 µs).
3. Average current consumption for RX startup (130 µs), and when changing mode from TX to RX (130 µs).

Maximum Power Consumption

Current consumption @ 1.8V	
Idle current, all blocks idle	3uA
Fast Advertising	1.2mA
Slow Advertising	0.18mA

Radio Characteristics

Symbol	Conditions	Min.	Typ.	Max.	Unit
Frequency	ISM Band	2400	_	2483.5	MHZ
Output Power		0		+4	dBm
Tx Power adjust step			4		dB
Modulation	GFSK				
Data Rate	On-air data rate	250K	1M	2M	bps
Receive Sensitivity	250Kbps,1Mbps, 1Mbps BLE		-90	-85	dBm

8. System Descriptions

CPU

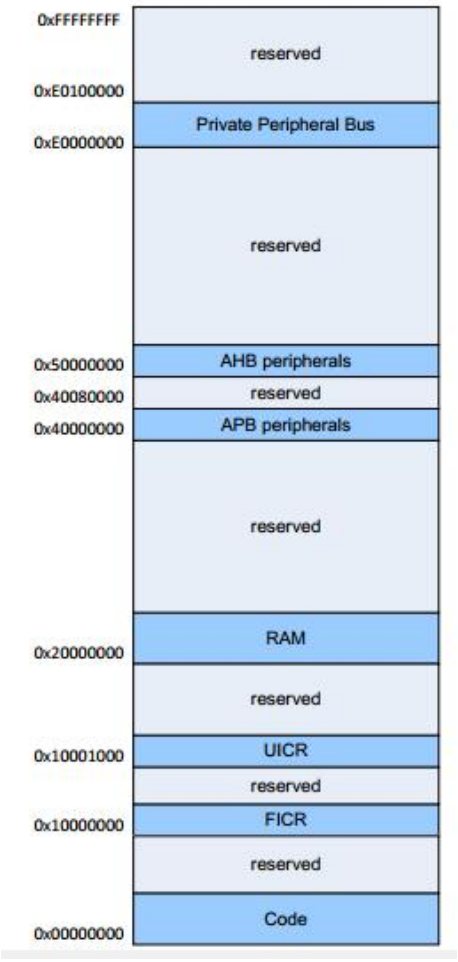
The ARM® Cortex™-M0 CPU has a 16 bit instruction set with 32 bit extensions (Thumb-2® technology) that delivers high-density code with a small-memory-footprint. By using a single-cycle 32 bit multiplier, a 3-stage pipeline and a Nested Vector Interrupt Controller (NVIC), the ARM Cortex-M0 CPU makes program execution simple and highly efficient.

The ARM Cortex Microcontroller Software Interface Standard (CMSIS) hardware abstraction layer for the ARM Cortex-M processor series is implemented and available for M0 CPU. Code is forward compatible with ARM Cortex M3 based devices.

Memory

All memory and registers are found in the same address space as shown in the Device Memory Map, see Figure 4. Devices in the nRF51 series use flash based memory in the code, FICR, and UICR regions.

The RAM region is SRAM



The embedded flash memory for program and static data can be programmed using In Application Programming (IAP) routines from RAM through the SWD interface, or in-system from a program executing from code area. The Non-Volatile Memory Controller (NVMC) is used for program/erase operations. It is also possible to set up the device to have readback protection on all or part of the code area by enabling readback protection in the UICR.

Power management

The power management system is highly flexible with functional blocks such as the CPU, Radio Transceiver, and peripherals having separate power state control in addition to the global System ON and OFF modes. In System OFF mode, RAM can be retained and the device state can be changed to System ON through reset or GPIO signal. When in System ON mode, all functional blocks will independently be In IDLE or RUN mode depending on needed functionality.

Power management features:

- System ON/OFF modes
- Brownout reset
- Power fail comparator
- Pin wake-up from System OFF
- Functional block RUN/IDLE modes
- 2-region RAM retention in System OFF mode

Programmable Peripheral Interconnect (PPI)

The Programmable Peripheral Interconnect (PPI) enables peripherals to interact autonomously with each other using tasks and events independent of the CPU. This feature allows precise synchronization between peripherals when application real-time constraints exist and eliminates the need for CPU activity to implement behavior which can be predefined using PPI.

Clock management (CLOCK)

The advanced clock management system can source the system clocks from a range of internal high and low frequency oscillators and distribute them to modules based upon a module's individual requirements. This prevents large clock trees being active and drawing power when no system modules needing this clock reference are active.

If an application enables a module that needs a clock reference without the corresponding oscillator running, the clock management system will automatically enable the RC oscillator option and provide the clock. When the module goes back to idle, the clock management will automatically set the oscillator to idle as well. To avoid delays involved in starting a given oscillator, or if a specific oscillator is required, the application can override the automatic oscillator management so it keeps oscillators active when no system modules require the clock reference.

GPIO

The Flexible general purpose I/O is organized as one port with up to 32 I/Os (dependant on package) enabling access and control of up to 32 pins through one port. Each GPIO can also be accessed individually and each has the following user configured features.

- Input/output direction
- Output drive strength
- Internal pull up and pull down resistors
- Wake-up from high or low level triggers on all pins
- Trigger interrupt on all pins
- All pins can be used by the PPI task/event system; the maximum number of pins that can be interfaced through the PPI at the same time is limited by the number of GPIOTE modules
- All pins can be individually configured to carry serial interface or quadrature demodulator signals

Debugger support

The 2-pin Serial Wire Debug (SWD) interface provided as a part of the Debug Access Port (DAP) in conjunction with the Nordic Trace Buffer (NTB) offers a flexible and powerful mechanism for non-intrusive debugging of program code. Breakpoints, single stepping, and instruction trace capture of code execution flow are part of this support.

2.4 GHz radio

The nRF51 series 2.4 GHz RF transceiver is designed and optimized to operate in the worldwide ISM frequency band at 2.400 to 2.4835 GHz. Radio modulation modes and configurable packet structure make the transceiver interoperable with Bluetooth® low energy (BLE), ANT™, Enhanced ShockBurst™, and other 2.4GHz protocol implementations.

The transceiver receives and transmits data directly toand from system memory for flexible and efficient packet data management.

Timer/counters (TIMER)

The TIMER timer/counter runs on the high-frequency clock source (HFCLK) and includes a 4 bit prescaler that can divide the HFCLK.

The extensive TIMER task/event and interrupt features make it possible to use the PPI system for timing/count tasks to/from any system peripheral including any GPIO of the device. The PPI system also enables the TIMER task/event features to generate periodic output and PWM signals to any GPIO. The number of input/ outputs used at the same time is limited by the number of GPIOTE modules.

Instance	Bit-width	Capture/Compare registers
TIMER0	32	4
TIMER1	16	4
TIMER2	16	4

Timer / Counter properties

Real Time Counter (RTC)

The Real Time Counter (RTC) module provides a generic, low power timer on the low-frequency clock source (LFCLK). The RTC features a 24 bit COUNTER, 12 bit (1/X) prescaler, capture/compare registers, and a tick event generator for low power, tickless RTOS implementation.

Instance	Capture/Compare registers
RTC0	4
RTC1	3

RTC properties

AES-ECB encryption (ECB)

The ECB encryption block supports 128 bit AES encryption. It can be used for a range of cryptographic functions like hash generation, digital signatures, and keystream generation for data encryption/decryption. It operates with EasyDMA access to system RAM for in-place operations on cleartext and ciphertext during encryption.

Random Number Generator (RNG)

The Random Number Generator (RNG) generates true non-deterministic random numbers based on internal thermal noise. These random numbers are suitable for cryptographic purposes. The RNG does not require a seed value.

Watchdog Timer (WDT)

A countdown watchdog timer using the low-frequency clock source (LFCLK) offers configurable and robust protection against application lock-up. The watchdog can be paused during long CPU sleep periods for low power applications and when the debugger has halted the CPU.

Temperature sensor

The temperature sensor measures die temperature over the temperature range of the device with 0.25°C resolution.

SPI

The SPI interface enables full duplex synchronous communication between devices. It supports a 3-wire (SCK, MISO, MOSI) bidirectional bus with fast data transfers to and from multiple slaves. Individual chip select signals will be necessary for each of the slave devices attached to a bus, but control of these is left to the application through use of GPIO signals. I/O data is double buffered.

The GPIOs used for each SPI interface line can be chosen from any GPIO on the device and are independently configurable. This enables great flexibility in device pinout and enables efficient use of printed circuit board space and signal routing.

Instance	Master/Slave
SPI0	Master
SPI1	Master

SPI properties

Two-wire interface (TWI)

The Two-wire interface can interface a bi-directional wired-AND bus with two lines (SCL, SDA). The protocol makes it possible to interconnect up to 128 individually addressable devices. The interface is capable of clock stretching and data rates of 100 kbps and 400 kbps are supported.

The GPIOs used for each Two-wire interface line can be chosen from any GPIO on the device and are independently configurable. This enables great flexibility in device pin-out and enables efficient use of board space and signal routing.

Instance	Master/Slave
TWI0	Master
TWI1	Master

Two-wire properties

UART (UART)

The Universal Asynchronous Receiver/Transmitter offers fast, full-duplex, asynchronous serial communication with built-in flow control (CTS, RTS) support in HW up to 1Mbps baud. Parity checking and generation for the 9th data bit are supported.

The GPIOs used for each UART interface line can be chosen from any GPIO on the device and are independently configurable. This enables great flexibility in device pinout and enables efficient use of board space and signal routing.

Quadrature Decoder (QDEC)

The quadrature decoder provides buffered decoding of quadrature-encoded sensor signals. It is suitable for mechanical and optical sensors with an optional LED output signal and input debounce filters. The sample period and accumulation are configurable to match application requirements.

Analog to Digital Converter (ADC)

The 10 bit incremental Analog to Digital Converter (ADC) enables sampling of up to 8 external signals through a front end multiplexer. The ADC has configurable input and reference prescaling, and sample resolution (8, 9, and 10 bit).

GPIO Task Event blocks (GPIOTE)

A GPIO TE block enables GPIOs on Port 0 to generate events on pin state change which can be used to carry out tasks through the PPI system. A GPIO can also be driven to change state on system events using the PPI system.

Instance	Number of GPIOs
GPIOTE	4

GPIOTE properties

9. Instance table

The peripheral instantiation of the nRF51822 is shown in the table below.

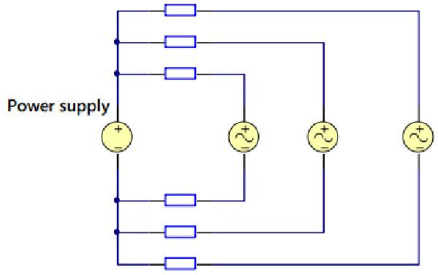
ID	Base address	Peripheral	Instance	Description
0	0x40000000	POWER	POWER	Power Control
0	0x40000000	CLOCK	CLOCK	Clock Control
1	0x40001000	RADIO	RADIO	2.4 GHz Radio
2	0x40002000	UART	UART0	Universal Asynchronous Receiver/ Transmitter
3	0x40003000	SPI	SPIM0	SPI0
3	0x40003000	TWI	TWI0	I2C compatible Two-Wire Interface 0
4	0x40004000	SPI	SPI1	SPI1
4	0x40004000	TWI	TWI1	I2C compatible Two-Wire Interface 1
5				Unused
6	0x40006000	GPIOTE	Port 0 Task and events	GPIO Tasks and events
7	0x40007000	ADC	ADC	Analog-to-Digital Converter
8	0x40008000	TIMER	TIMER0	Timer/Counter 0
9	0x40009000	TIMER	TIMER1	Timer/Counter 1
10	0x4000A000	TIMER	TIMER2	Timer/Counter 2
11	0x4000B000	RTC	RTC0	Real Time Counter 0
12	0x4000C000	TEMP	TEMP	Temperature Sensor
13	0x4000D000	RNG	RNG	Random Number Generator
14	0x4000E000	ECB	ECB	Crypto AES ECB
15	0x4000F000	CCM	CCM	AES Crypto CCM
15	0x4000F000	AAR	AAR	Accelerated Address Resolver
16	0x40010000	WDT	WDT	Watchdog Timer
17	0x40011000	RTC	RTC1	Real Time Counter 1
18	0x40012000	QDEC	QDEC	Quadrature Decoder
19				Unused
20				Reserved as software input
21				Reserved as software input
22				Reserved as software input
23				Reserved as software input
24				Reserved as software input
25				Reserved as software input
26				Unused
27				Unused
28				Unused
29				Unused
30	0x4001E000	NVMC	NVMC	Non-Volatile Memory Controller
31	0x4001F000	PPI	PPI	Programmable Peripheral Interconnect
NA	0x50000000			General Purpose Input and Output
NA	0x10000000	FICR	FICR	Factory Information Configuration Registers
NA	0x10001000	UICR	UICR	User Information Configuration Registers

10. Layout Guide

- Place the module as close as the mother board edge.
- Never place ground plane or tracks underneath the antenna area.
- Never place the antenna very close to metallic objects.

Layout for high performance

- Locate the antenna as far away as possible from the user's body.
- Do not put the antenna inside a metal enclosure or metalized plastic casing.
- Use a 50 ohm track for RF transmission line (for none Antenna Module)
- Uses the ground plane on RF transmission side (for none Antenna Module)
- Better power routing

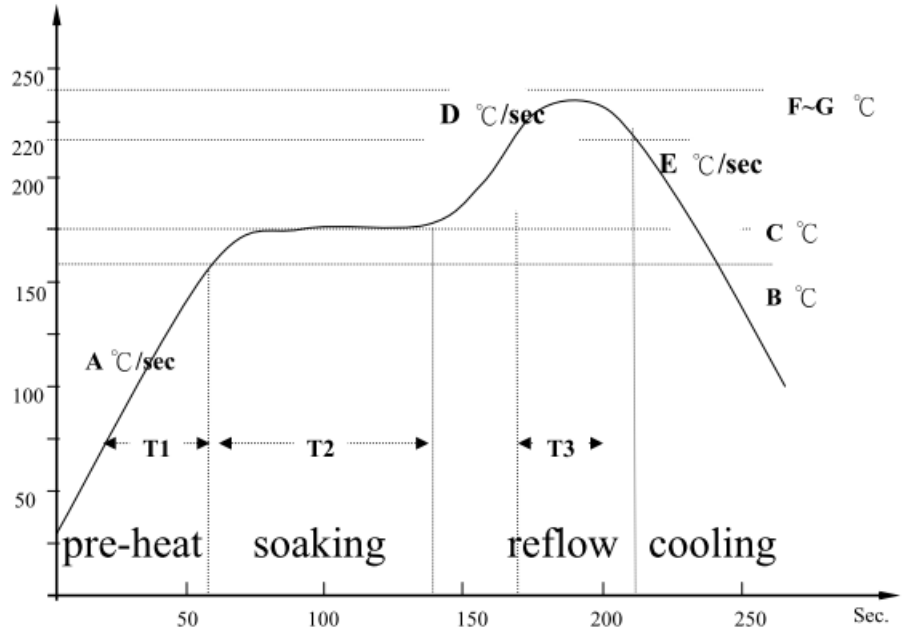


Star routed

- Components with high current draw must have its own track to the power supply.
- Decupling capacitors must be placed as close as possible to power supply pin.
- Decupling capacitors must Local ground plane with several vias.
- Decoupling capacitors close to noisy components
- Make sure all ground planes are connected with lots of vias.
- Ground plane between I/O-tracks.
- Low impedance ground plane.
- Refer the recommend solder pads dimension page and for correct layout procession.

11. Soldering Profile

Temperature Profile



A: ramp up rate during preheat: 1.0~3.0 ℃/sec (Best: 1.5~2.0 ℃/sec)

B~ C : soaking temperature: 155~185 ℃

D: ramp up rate during reflow: 1.2~2.3 ℃/sec

E: ramp down rate during cooling: 1.0~3.0 ℃/sec (Best: 1.7~2.2 ℃/sec)

F~G : peak temperature: 240~250℃

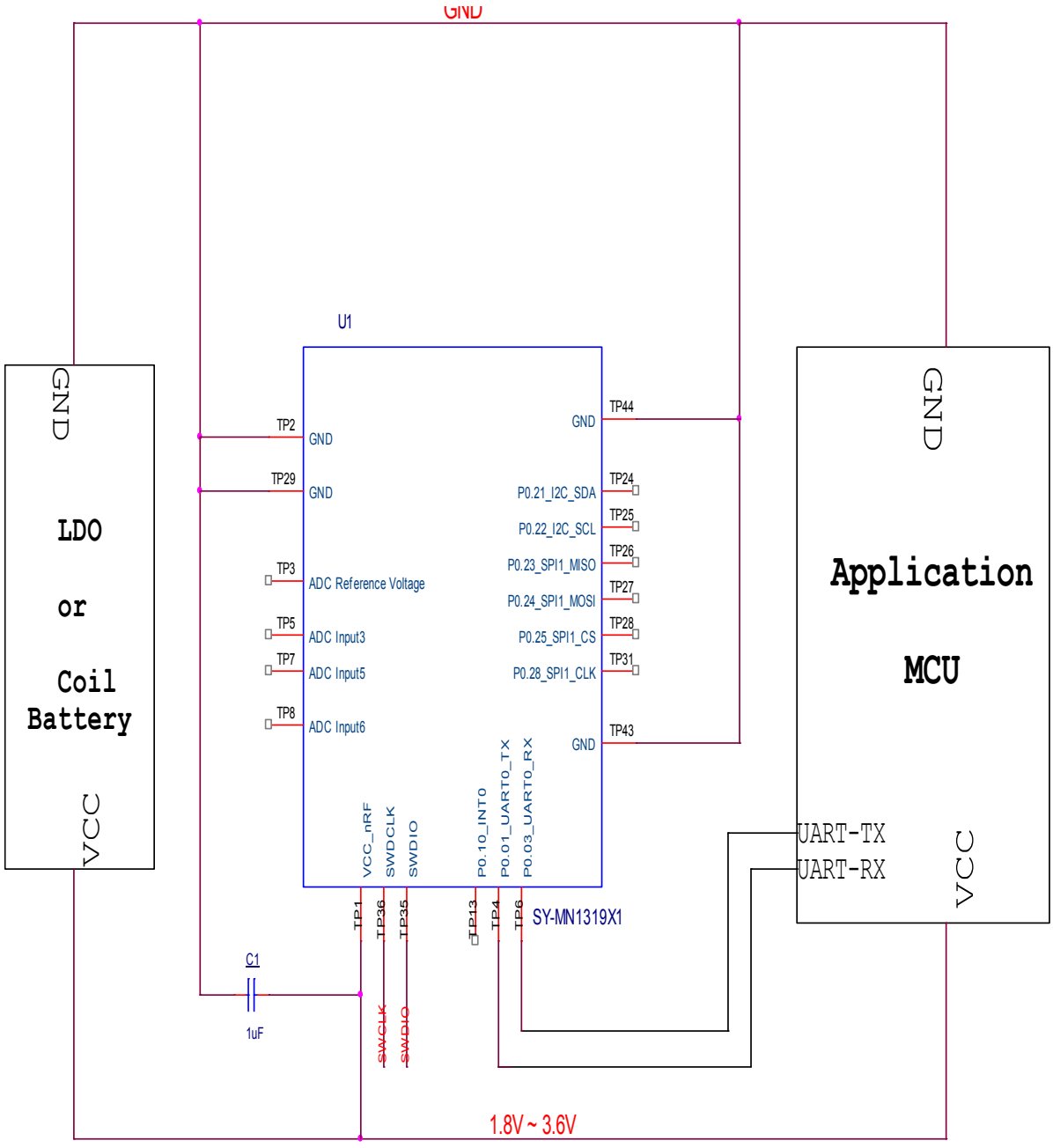
T1: preheat time: 50~80 sec

T2 : dwell time during soaking: 100~110 sec

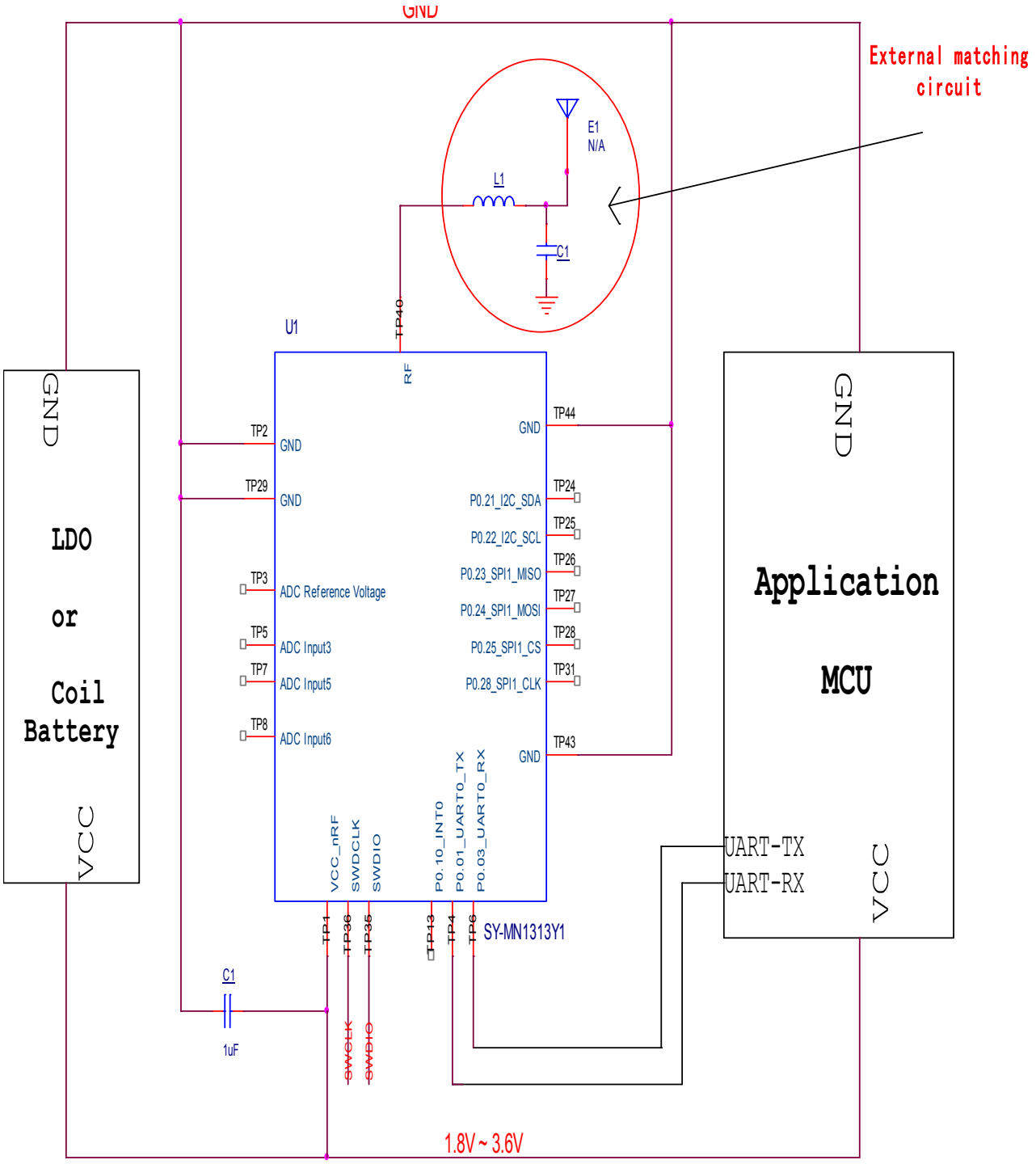
T3 : time above 220 ℃ : 60~70 sec(Max: 100sec)

12. Reference Schematic

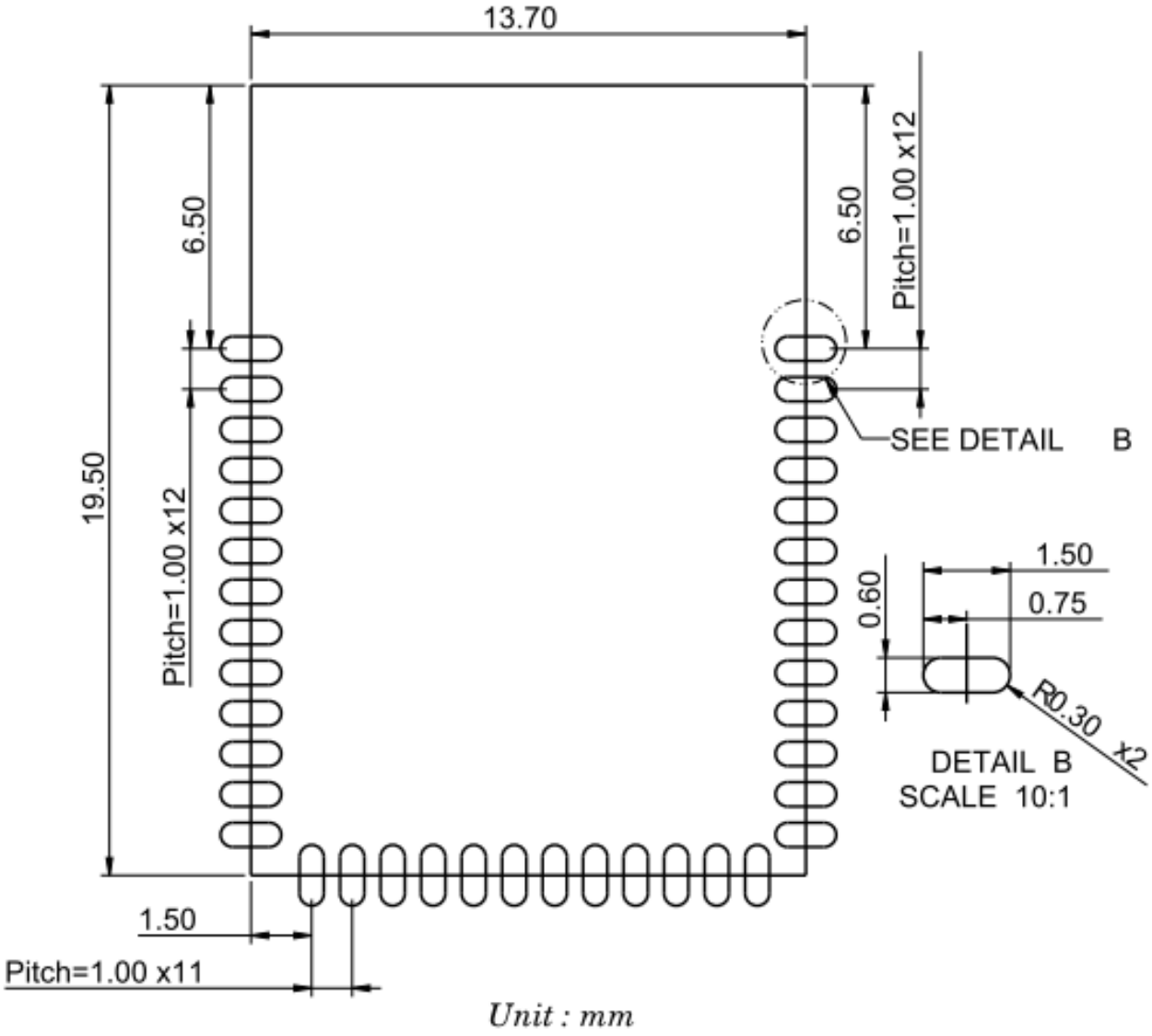
Embedded Antenna



None Antenna



13. Recommended of PCB Layout Pads



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